Digital Logic Design Laboratory

Lab 6

Flip Flops and Counters

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Class: ……………………………………………….......

Date: …………………………………………………....

# I. Objectives

In this laboratory, students will study:

- Understand the operation of Flip Flops.

- Use a Flip Flops and design/implement a circuit based on a function definition.

- Design a counter based on Flip Flops

# II. Procedure

1. Investigate Flip Flops (FF)

Flip flops are one of the most fundamental electronic components. These are used as one-bit storage elements, clock dividers and it can make counters, shift registers and storing registers by connecting the flip flops in particular sequences.

a. JK- Flip Flops

Given the JK Flip Flop as shown in Figure 1. The J-K flip-flop is the most versatile of the basic flip-flops. It has two inputs, traditionally labeled J and K. If J and K are different then the output Q takes the value of J at the next clock edge.

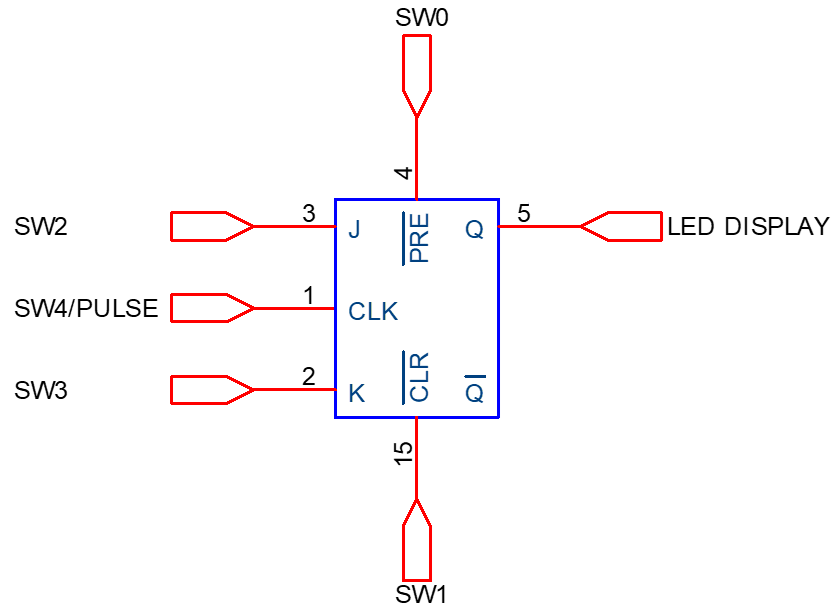


Figure 1. JK Flip Flop

Built the truth table:

|  |  |  |  |
| --- | --- | --- | --- |
| J | K | CLK | Q+ |
| 0 | 0 | ↓ | No change |
| 0 | 1 | ↓ | 0 |
| 1 | 0 | ↓ | 1 |
| 1 | 1 | ↓ | Toggle |

What is the usage of  and ?

used to set the output to HIGH regardless of the state of the clock

used to set the output to LOW, or “reset” the output Q to zero, regardless of clock’ state

Implement the circuit (Figure 1) via simulation software and paste the result in here

A computer screen shot of a diagram

Description automatically generated

b. D- Flip Flops

The D flip-flop tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell.

Diagram, schematic

Description automatically generated

Figure 2. D Flip Flop

Built the truth table:

|  |  |  |
| --- | --- | --- |
| D | CLK | Q+ |
| 0 | ↑ | 0 |
| 1 | ↑ | 1 |

What is the usage of  and ?

used to set the output to HIGH regardless of the state of the clock

used to set the output to LOW, or”reset” the output Q to zero, regardless of clock’s state.

Implement the circuit (Figure 2) via simulation software and paste the result in here

A computer screen shot of a diagram

Description automatically generated

c. Convert JK-FF into D-FF

From the block diagram shown in figure 3, design the circuit to convert JK-FF to D-FF:

Diagram

Description automatically generated

Figure 3. Convert JK-FF into D-FF

Implement the circuit via simulation software and paste the result in here

A computer screen shot of a diagram

Description automatically generated

Make comment on the results

By setting J=D and K=D' in a JK Flip-Flop, it behaves like a D Flip-Flop. This simplifies control since D Flip-Flop has only one input to manage, making it easier for circuit design and management.

2. Analyze and design asynchronous counters

a. Implement an asynchronous up counter having M = 8 using J-K Flip Flop

Implement the below circuit in Figure 4. Control  (SW1) and (SW2) to make the circuit operate.

Diagram, schematic

Description automatically generated

Figure 4. Logic diagram

Implement the circuit via simulation software and paste the result in here

A computer screen shot of a computer circuit

Description automatically generated

Make comment on the results

This asynchronous counter, designed with three JK Flip-flops, effectively counts from 0 to 7 upon receiving eight clock pulses. It exhibits the 'ripple' effect, where state changes sequentially propagate through the flip-flops. While simple and suitable for low-speed operations, it can present timing issues at higher speeds due to this ripple delay.

b. Design an asynchronous up counter having M = 6 by using J-K Flip Flop

Show the way to make it (step by step)

Step 1: Determine the flip-flops will be used for given M=6

MOD-N: counter contains N-states => 5 states run form 0-5

For these given values, so we need at least 3 Flip-Flops .

Step 2: Determine the number of states of MOD-6: 000-001-010-011-100-101-back to 000. We force 110 to be 000 => Q2’Q1’Q’

Step 3: Write the truth table of MOD-6 asynchronous counter:

|  |  |  |  |
| --- | --- | --- | --- |
| Decimal number | Q1 | Q2 | Q3 |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| SET to 0 | Q1` | Q2` | Q3` |

Y = Q1` + Q2` + Q3`

Step 4: Using logic gate to implement the circuit

Implement the circuit via simulation software and paste the result in here

A computer screen shot of a computer circuit

Description automatically generated

Make comments on the results:

The implementation of an asynchronous up counter with M=6 using three JK Flip-Flops is successful. The counter effectively cycles through states, counting from 0 to 5 in binary, and resets when reaching state 6. This demonstrates the correct operation of the MOD-6 counter.

c. Implement an asynchronous 3-bit down counter having M = 8 by using J-K Flip Flop

Implement the below circuit shown in Figure 5. The  (SW1) and (SW2) inputs are in the appropriate states to make the circuit operate:

Diagram, schematic

Description automatically generated

Figure 5. Logic diagram

Implement the circuit via simulation software and paste the result in here

A computer screen shot of a circuit

Description automatically generated

Make comment on the results

The asynchronous 3-bit down counter effectively counts from 7 to 0 using three JK Flip-Flops. This design is successful in creating a ripple effect where changes in state propagate through the flip-flops.

d. Implement an asynchronous 3-bit counter having M = 8, with a control for up/down counting.

Implement the below circuit shown in Figure 6. The  (SW1) and (SW2) inputs are in the appropriate states to make the circuit operate:

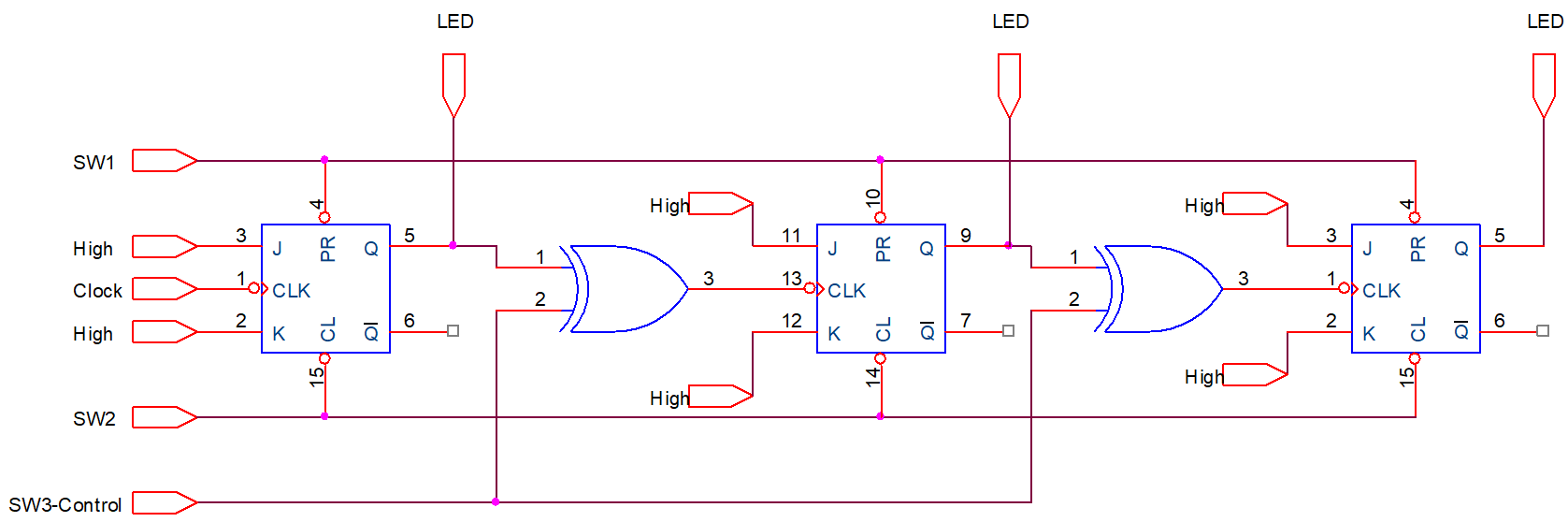


Figure 6. Logic diagram

Implement the circuit via simulation software and paste the result in here

Make comment on the results

3. Analyze and design synchronous counters

a. Analyze the counter given schematic circuit

Implement the below circuit in Figure 7. Control  (SW1) and (SW2) to make the circuit operate.

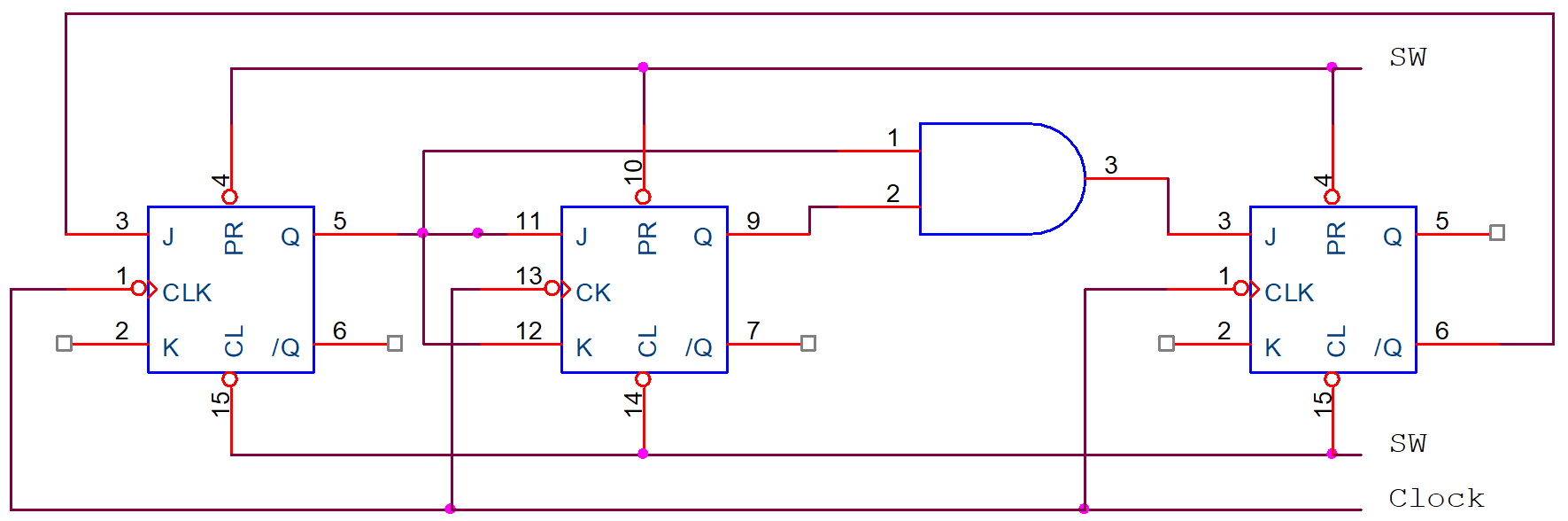


Figure 7. Logic diagram

When the clock is active:

…………………………………………………………………………………………………………………………………………………………………………………….

Write the excitation (trigger) input equations of all flip-flops:

J0 = …………………...............; K0 = ….……………...............

J1 = …………………...............; K1 = ….……………...............

J2 = …………………...............; K2 = ….……………...............

Transition Table

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | | |  | | | | | | Next State | | |
| Q2 | Q1 | Q0 | J2 | K2 | J1 | K1 | J0 | K0 | Q2 | Q1 | Q0 |
| 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |
| 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |
| 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |
| 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |
| 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |
| 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |
| 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |

Implement the circuit via simulation software and paste the result in here

Draw the state diagram of the counter

Make comment on the results

b. Design and implement a synchronous counter by the given state diagram

Design and implement a synchronous 2-bit counter shown in the given diagram as shown in Figure 8 using J-K Flip Flops

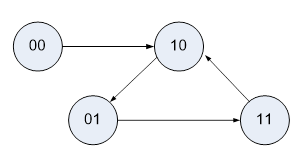


Figure 8. State diagram

Transition Table

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | |  | | | | Next State | |
| Q1 | Q0 | J1 | K1 | J0 | K0 | Q1 | Q0 |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |

Write the excitation (trigger) input equations of all flip-flops:

J0 = …………………...............; K0 = ….……………...............

J1 = …………………...............; K1 = ….……………...............

Implement the circuit via simulation software and paste the result in here

Make comment on the results